

- 1           1.    A method comprising:  
2                   forming a metal oxide semiconductor field effect  
3 transistor having an epitaxially deposited source/drain  
4 that extends under the edges of a gate electrode.
  
- 1           2.    The method of claim 1 including forming a  
2 source/drain extension that extends under the edges of a  
3 gate electrode.
  
- 1           3.    The method of claim 1 including forming a  
2 sacrificial epitaxially deposited material over a substrate  
3 and forming a gate electrode over said epitaxially  
4 deposited layer.
  
- 1           4.    The method of claim 3 wherein forming a  
2 sacrificial epitaxially deposited material includes  
3 epitaxially depositing a silicon material.
  
- 1           5.    The method of claim 3 including selectively  
2 etching said epitaxially deposited material.
  
- 1           6.    The method of claim 5 including using sonication  
2 to selectively etch said material.

1        7.    The method of claim 3 including forming a  
2    sidewall spacer on said gate electrode and etching under  
3    said sidewall spacer.

1        8.    The method of claim 5 including selectively  
2    etching said epitaxially deposited material so as to  
3    undercut said gate electrode.

1        9.    The method of claim 8 including depositing an  
2    epitaxial material on said substrate and extending under  
3    said gate electrode.

1        10.   The method of claim 9 including forming a doped  
2    epitaxial material.

1        11.   The method of claim 8 including forming said  
2    epitaxial material to be thinner near the gate electrode  
3    and thicker spaced from said gate electrode.

1        12.   The method of claim 1 including forming a delta  
2    doped transistor.

1        13.   A field effect transistor comprising:  
2                a substrate;  
3                a doped epitaxial semiconductor material formed  
4    over said substrate; and

5           a gate electrode formed over said doped epitaxial  
6 semiconductor material, said doped epitaxial semiconductor  
7 material extending under said gate electrode.

1           14. The transistor of claim 13 including a  
2 source/drain having a source/drain extension, said  
3 source/drain extension being formed of said doped epitaxial  
4 semiconductor material and extends under the edges of the  
5 gate electrode.

1           15. The transistor of claim 14 wherein said material  
2 has a first thickness near said gate electrode and a second  
3 thickness spaced from said gate electrode, said second  
4 thickness being greater than said first thickness.

1           16. The transistor of claim 15 including a sidewall  
2 spacer, said material extending under said sidewall spacer.

1           17. The transistor of claim 16 wherein said second  
2 thickness is aligned with said sidewall spacer.

1           18. The transistor of claim 13 wherein said  
2 transistor is a delta doped transistor.

1        19. The transistor of claim 13 including an ion  
2 implanted source/drain under said doped epitaxial  
3 semiconductor material.

1        20. A method comprising:  
2            forming a epitaxial semiconductor layer over a  
3 semiconductor substrate wherein the epitaxial semiconductor  
4 layer has a lower doping concentration than the substrate;  
5            forming a gate structure including a gate  
6 electrode and a sidewall spacer over said epitaxial  
7 semiconductor layer; and  
8            selectively etching the exposed portion of said  
9 epitaxial semiconductor layer as well as a portion of said  
10 epitaxial semiconductor layer under said gate electrode.

1        21. The method of claim 20 including epitaxially  
2 depositing a doped semiconductor material over said  
3 substrate to fill the region under said gate electrode and  
4 under said sidewall spacer.

1        22. The method of claim 21 wherein said epitaxial  
2 semiconductor layer has a first thickness under said gate  
3 electrode and a second thickness spaced from said gate  
4 electrode.

1        23. The method of claim 22 including forming said  
2 second thickness in alignment with said spacer.

1        24. The method of claim 20 including forming a deep  
2 source/drain region by ion implantation.

1        25. The method of claim 20 including forming said  
2 epitaxial semiconductor layer extending under said gate  
3 electrode and having a greater thickness outbound of said  
4 gate electrode and a lesser thickness under said gate  
5 electrode.